

# CMOS Active Pixel Sensor (APS) Imager for Scientific Applications

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## ABSTRACT

A 512x512 CMOS Active Pixel Sensor (APS) imager has been designed, fabricated, and tested for frontside illumination suitable for use in astronomy specifically in telescope guider systems as a replacement of CCD chips. The imager features a high-speed differential analog readout, 15  $\mu\text{m}$  pixel pitch, 75 % fill factor (FF), 62 dB dynamic range, 315Ke- pixel capacity, less than 0.25% fixed pattern noise (FPN), 45 dB signal to noise ratio (SNR) and frame rate of up to 40 FPS. Design was implemented in a standard 0.5  $\mu\text{m}$  CMOS process technology consuming less than 200mWatts on a single 5 Volt power supply.

CMOS Active Pixel Sensor (APS) imager was developed with pixel structure suitable for both frontside and backside illumination holding large number of electron in relatively small pixel pitch of 15  $\mu\text{m}$ . High-speed readout and signal processing circuits were designed to achieve low fixed pattern noise (FPN) and non-uniformity to provide CCD-like analog outputs. Target spectrum range of operation for the imager is in near ultraviolet (300-400 nm) with high quantum efficiency. This device is going to be used as a test vehicle to develop backside-thinning process.

Keywords: CMOS APS, active pixel sensor, image sensor, scientific imager, backside illumination, guider, UV sensor.

## 1. INTRODUCTION

Much effort has been devoted on research and development of solid-state image sensors driven preliminarily by consumer electronics products such as camcorders, and digital PC and commercial cameras in the last couple of decades. Increasing market demand on larger pixel numbers, better quality, low power, low cost, small footprint, less supporting electronics and most importantly the compatibility of mainstream VLSI fabrication technology are the main driving forces for these activities.

Charge Coupled Devices (CCDs) have been the unequalled leaders in the fields of electronic imaging for all kinds of applications for a long time. They are widely used and mature with respect to production yield and performance. In the last decade, a relatively new photon sensing image array, Active Pixel Sensor (APS), has emerged as a potential replacement to CCDs. The APS chips utilize existing Complementary Metal Oxide Semiconductor (CMOS) production facilities. The APS technology preserves all the desirable features of CCDs, yet circumvents the major weaknesses of the CCD technology. APS technology has several advantages over CCD technology, including; lower cost, lower power consumption (100 to 1000 times lower), higher dynamic range, higher blooming threshold, individual pixel readout, single low voltage (5, 3.3, or lower) operation, high speed, large array sizes, radiation hardness, and the smartness by incorporating on-chip signal processing.

High-resolution imaging applications such as professional electronic still photography, astronomical imaging, x-ray imaging, TV broadcasting and machine vision requires large format image sensors. CCDs have been fabricated with very large array formats to support these emerging markets. 66 Million-pixel (7Kx9K) front-illuminated CCD with 12  $\mu\text{m}$  pixel<sup>1</sup>, and 85 Million-pixel (9Kx9K) wafer scale CCD with 8.75  $\mu\text{m}$  were introduced in 1997, and 1999 respectively<sup>2</sup>. However, large format CCDs are extremely expensive and difficult to produce with the low defect densities needed for quality imaging. As the desire

for increased well-depth, and spectral response are added, the necessary increase in pixel size (and hence, sensor size) makes the production of such a CCDs prohibitively expensive. Furthermore, the power consumption and need for external support circuitry make CCDs considerably less attractive for earth-based, or space-borne applications. CMOS APS technology gained more popularity by the recent advancement in the frame rate<sup>3,4</sup> and array formats in this part of the image sensor market.

Spectral response of an imager is directly related to the physical and spectral properties of the sensing element. For example in the UV and soft X-ray spectrums front illuminated CCDs are insensitive because of the absorption at the front layers. Backside illumination is being used with some success to extend and enhance the spectral response of CCD in UV<sup>5</sup>. However, a truly satisfactory backside thinning, passivation, UV enhancement, packaging, and long term stability issues of these devices has prevented their widespread use in UV applications. Currently in UV spectrum applications, low quantum efficiency (QE), low-modulation transfer function (MTF), down converting phosphors (lumogen, metachrome, etc.) deposited on the frontside (or backside) of CCDs are used. UV response in spaceborne telescopes is of great interest and improving the UV response of CCDs has been an area of lots of activity<sup>6</sup>. Yet, UV spectrum and backside illumination still remain uncharted territories for CMOS APS technology.

## 2. CMOS APS DESIGN

CMOS APS chip composes of CMOS a 512 x 512 active pixel sensor (APS) array, row timing generators for row shift registers to set reset and read pointers on the pixel array, row drivers, column analog signal processors (ASPs) containing column buffers, offset cancellation and sample and hold (S/H) circuits, column shift registers controlled by column clock and timing generator, global charge and sample and hold (S/H) amplifiers, and analog/digital buffers as shown in the Fig. 1.

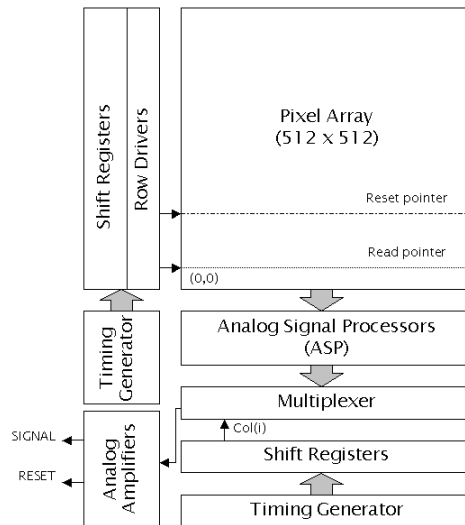


Fig. 1. Block Diagram of the CMOS APS

Standard photodiode type CMOS active pixel sensor (APS) was used. It composes of three NMOS transistors and a photo-conversion site or photodiode (PD) as shown in the Fig. 2. One source follower amplifier is used in each pixel. Upper half of the source follower ( $M_{sf}$ ) is located in the pixel while lower half of it ( $M_{vln}$ ) is shared by a column of pixels that were connected to the common column bus.  $M_{vln}$  transistor is biased at operation point of the source follower amplifier creating constant current sink. Extra two transistors are placed in between two source follower transistors. One is located in the pixel ( $M_{sel}$ ), and is activated by row decoder during the pixel read period, and the other one located at the bottom of the column bus ( $M_{vlnen}$ ). These transistors are turned on during pixel readout time, and turned off after the pixel signals were sampled. APS pixel operates in integration mode requiring frequent reading and resetting

of the photodiode (PD) nodes. Pixel is reset right before the integration time starts through the reset transistor (Mrst). Reset pulse (RST) is produced by row decoder, and driven by row driver to the entire row of pixels. Photodiode node is typically reset to supply voltage (VAA\_PIX) when reset pulse activated providing known photodiode signal level. During the integration time, photo-generated electrons in the photodiode node discharge the node capacitance providing a light proportional signal level at the end of the integration time. After the integration time ends, a row of pixels are selected, and the content of the photodiode is buffered through the pixel buffer to the column analog signal processor (ASPs).

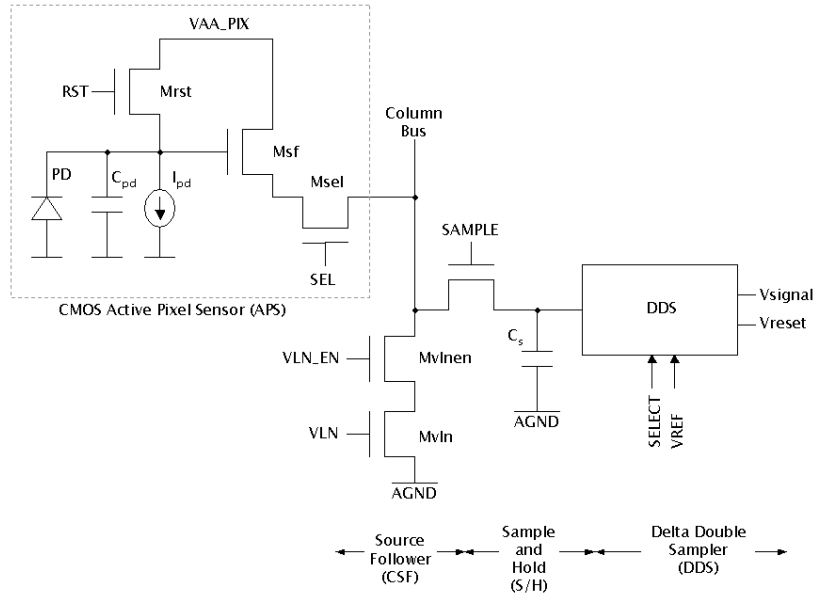


Fig. 2. Schematic diagrams of the CMOS APS pixel and column analog signal processor (ASP).

Analog signal processor (ASP) composes of column source follower (CSF), a sample and hold (S/H) circuit and delta double sampling (DDS) circuits (Fig. 2). DDS circuit composes of a p-type source follower and two charge mode sampling capacitances, and two column select transistors. DDS circuits are used as level shifter and reduce the fixed pattern noise (FPN). Also it conditions sampled voltage domain signals for charge domain global readout circuits. ASP control signals are generated in the column shift register, and column timing generator circuits. Column shift registers select column ASPs sequentially during column readout period. Stored differential charges in the ASPs are transferred to two global charge amplifiers, and driven off chip. Each channel composes of one charge amplifier, one sample and hold (S/H) circuit and an output buffer amplifier. Column timing generator generates control signals of the global charge amplifiers.

There are three gain stages from pixel photodiode node to the chip outputs, as shown in the Fig. 3. Pixel source follower is the first gain stage and has a typical gain between 0.7 and 0.8. Analog signal processor contains another gain stage that conditions the signal from first gain stage to the next. Global signal amplifiers contain charge amplifier and the output buffer.

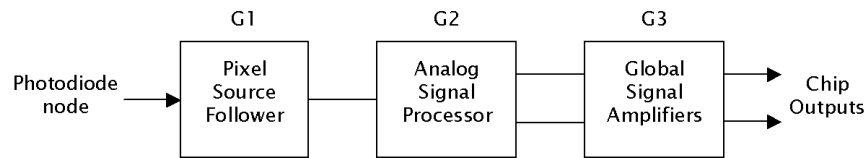


Fig. 3. Signal chain from pixel node to chip outputs

Total gain of the signal chain from photodiode node to output ports was fixed to 1.0 (Volt/Volt), and was measured  $1.0 \text{ (V/V)} \pm 5\%$  for the design.

### 3. MEASUREMENT AND CHARACTERIZATION

Free electrons are generated mainly by process related parameters like impurities, stress, material boundaries in the substrate, and proton irradiation damage that cannot be separated from photo-generated electrons in the pixel. These electrons are called dark current, as they generate a background signal, even when the imager is not illuminated. Dark current generation is non-uniform over the imager array, leading to a fixed offset pattern in the resulting image. In integrating imagers, such as CMOS APS and CCD, the amplitude of this additional non-uniformity is proportional to the integration time.

Dark current generation also is a stochastic process, and as such is a source of shot noise. This leads to a dark current induced temporal noise component equal to the square root of the amount of dark electrons generated in a pixel. When imaging faint scenes with an integrating imager, the accumulation of dark electrons puts a limit to the allowable duration of exposure, before the pixel's capacity saturates.

Dark current can be specified as a number of input referred electrons generated per second in a pixel, or as a current per area unit. It is measured by plotting average pixel output voltage levels at different integration times while the imager places in a dark and controlled temperature environment. The slope of the plot is used to calculate the dark current. If the conversion gain and pixel pitch of the imager is known, dark current is converted to ampere per squared area, or to electron per second. Dark current was measured at different integration time as shown in the Fig. 4. Measured dark current was  $32.75 \text{ mVolt/sec}$ .

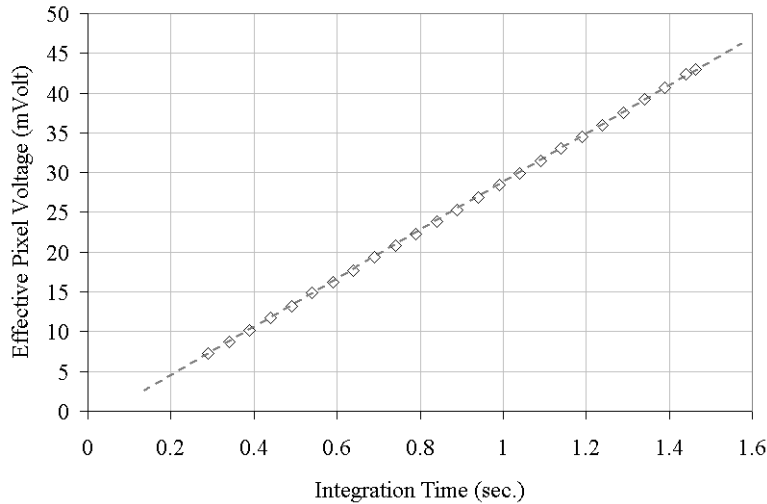


Fig. 4. Measured dark current.

One of the most important parameter regarding the characterization of photon detectors is the determination of the signal generated per photo electron known as the conversion gain (G) and is defined by<sup>7</sup>

$$G = \frac{\partial x}{\partial(\eta \cdot \Phi)} \quad [\mu\text{Volt}/e^-]$$

where  $\eta$  is the quantum efficiency (photoelectrons per incident photo),  $\Phi$  is the number of incident photons during the detector's integration period, and  $x$  is the detector's signal in appropriate units (e.g., mVolt). Using the Poisson statistics this equation can be written as;

$$G = \frac{\sigma^2}{\bar{x}} \quad [\mu\text{Volt}/e^-]$$

where  $\sigma$  is the variance of the detector's signal, and  $\bar{x}$  is the mean value of the detector's signal. The trace of  $\sigma$  versus  $\bar{x}$  is called photon transfer curve.

Measurement is done by stepped the light source from complete darkness to full well illumination in precisely measured increments. At each illumination level, typically 30 to 60 frames are captured and the mean and variance are computed. The exact illumination level for each measurement is recorded with a calibrated photodiode. Conversion gain is then computed by getting the slope of the photon transfer curve in the photon shot noise limited region. Variance and the mean values are calculated by using the following formulas.

$$\text{Mean} \quad : \quad \bar{x} = \frac{1}{T} \cdot \sum_{k=0}^T \bar{x}_k \quad [\text{mVolt}]$$

$$\text{Variance} \quad : \quad \sigma^2 = \frac{1}{M \cdot N} \cdot \sum_{i=0}^M \sum_{j=0}^N \sigma^2(i, j) \quad [\text{mVolt}^2]$$

where  $\bar{x}_k$ , and  $\sigma^2(i, j)$  are

$$\bar{x}_k = \frac{1}{M \cdot N} \cdot \sum_{i=0}^M \sum_{j=0}^N x_k(i, j) \quad [\text{mVolt}]$$

$$\sigma^2(i, j) = \frac{1}{T} \cdot \sum_{k=0}^T (x_k(i, j) - \bar{x}_k)^2 \quad [\text{mVolt}^2]$$

where  $i$  and  $j$  are the coordinates of a pixel,  $T$  is the number of frames that were collected,  $\bar{x}_k$  and is the mean signal value of the frame  $k$ .  $\sigma^2(i, j)$  is the variances of a pixel over  $T$  frames,  $M$  and  $N$  are the width and height of the calculation window. Photon transfer curve of the CMOS APS chip was measured collecting 64 frames at 65msec integration time. It is shown in the Fig. 5. Measured noise floor of the chip is 0.85mVolt with 6.7  $\mu\text{Volt}/e^-$  conversion gain. Measured pixel full well capacity was 315Ke-.

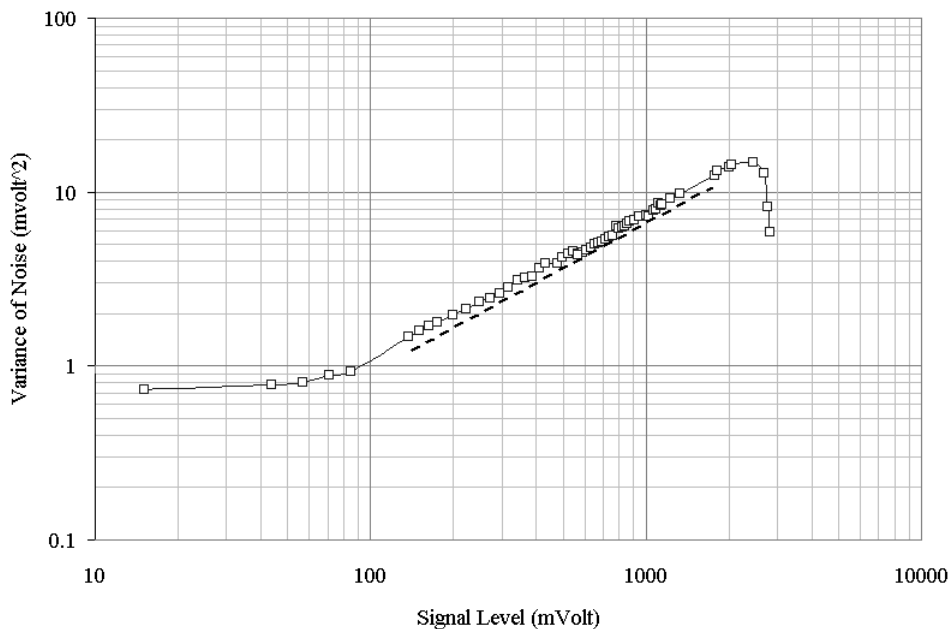


Fig. 5. Photon Transfer Curve

Other parameters were measured and tabulated in the Table 1. PGA84L type package was used for the design. Microphotograph of the designed CMOS APS chip is shown in the Fig. 6.

Table 1. Characterization results of the CMOS APS imager

|                             |                                 |
|-----------------------------|---------------------------------|
| Array Size                  | 512 x 512                       |
| Pixel Pitch                 | 15 $\mu\text{m}$                |
| Pixel Type                  | Photodiode APS                  |
| Pixel Fill Factor           | 75%                             |
| Technology                  | 0.5 $\mu\text{m}$ CMOS (2P3M)   |
| Output Format               | Differential Analog             |
| Frame Rate (up to)          | 40FPS                           |
| Gain                        | 1.0 V/V                         |
| Responsivity at 550 nm      | 2 Volt/Lux.sec                  |
| Linearity                   | < 5% of Signal                  |
| Noise Floor                 | 850 $\mu\text{Volt}$            |
| Saturation                  | 2.10 Volt<br>315,000 e-         |
| Conversion Gain             | 6.7 $\mu\text{Volt}/\text{e-}$  |
| Fixed Pattern Noise (FPN)   | < 0.25 (% Vsat)                 |
| Signal-to-Noise Ratio (SNR) | 46.5 dB                         |
| Dynamic Range               | 62 dB (@Vsat)                   |
| Dark Signal                 | < 33 mVolt/sec<br>< 5000 e-/sec |
| PRNU                        | < 0.23 (% Vsat)                 |
| Power Supply                | 5 Volt                          |
| Power Consumption           | < 200 mWatts                    |
| Package                     | PGA 84L                         |
| Chip Size                   | 9.75 mm x 9.75 mm               |

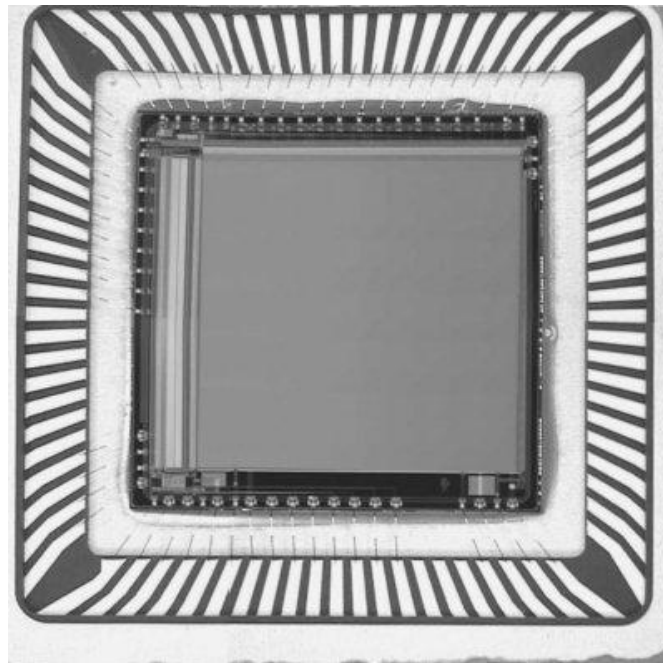


Fig. 6. Microphotograph of the CMOS APS chip.

#### 4. BACKSIDE ILLUMINATED CMOS APS

Modern CMOS chips compose of multi layers of metalization, passivation, and other filling material on top of the silicon substrate. Typically, optical properties of these multi layer structures are not optimized for image sensors. Due to the optical properties of these layers most of the impinging photons bounce back to the space and fraction of the photons can be reach to pixel collection area. This reduces the quantum efficiency of the frontside-illuminated imagers. These problems were eliminated by process modifications such as layer index optimization and antireflection coating in CCD technologies. Other optimization techniques were also used to improve quantum efficiency of the CCDs for frontside illumination such as open pinned phase (OPP) CCD<sup>8</sup>, thin-gate CCD<sup>9</sup>, and transparent-gate CCD<sup>10</sup>. However, these techniques may not be implemented in standard CMOS processes due to the required extra production and development costs. Post fabrication processes are more likely path to improve quantum efficiency of the frontside illuminated CMOS imagers. Antireflection (AR), and phosphor coating are two techniques widely used in frontside illuminated CCDs that well suits for CMOS APS devices. Other method is backside thinning and illumination of the CMOS device as shown in the Fig. 7.

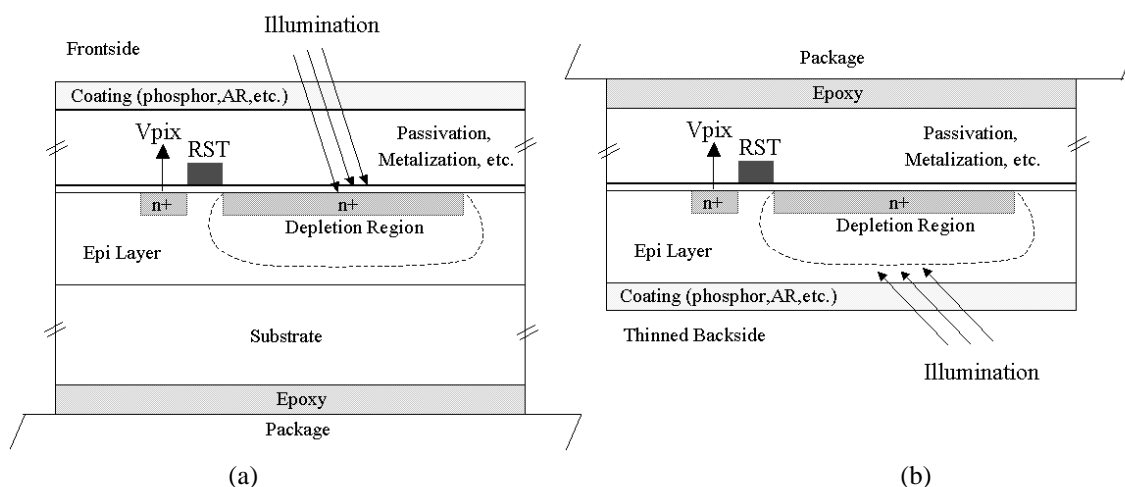


Fig. 7. Layer structure of a typical CMOS APS pixel for (a) frontside, and (b) backside illumination.

We are going to use the designed CMOS APS chip to develop a backside illuminated CMOS APS device. Development of this is still underway.

#### 5. CONCLUSION

A CMOS APS imager was designed, and characterized for frontside illumination. Designed imager composes of 512 x 512 photodiode type CMOS APS pixels with 15  $\mu\text{m}$  pitch. Imager has one differential analog output port working up to 40 FPS frame rate. This device is going to be used as a test vehicle to develop a backside thinning procedure.

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